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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/993,779	11/05/2001	Hakan Ozdemir	01-S-046 (1678-48)	7603
30431 7590 01/30/2007 STMICROELECTRONICS, INC. MAIL STATION 2346 1310 ELECTRONICS DRIVE CARROLLTON, TX 75006			EXAMINER RODRIGUEZ, GLENDA P	
			ART UNIT	PAPER NUMBER
			2627	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

09/993,779

Applicant(s)

OZDEMIR, HAKAN

Examiner

Glenda P. Rodriguez

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 October 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5,21-42,49 and 50 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5,21-42,49 and 50 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakane et al. (US Patent No. 6, 091, 699).

Regarding Claim 1, Nakane et al. teaches a head-connection-polarity detector, comprising:

A circuit operable to recover servo data from a servo signal generated by a read-write head that is coupled to the circuit with a connection polarity (See Fig. 4, wherein the drawing discloses a circuit that tracks the servo polarity in the disk.); and

A determinator coupled to the circuit and operable to determine the connection polarity from the recovered servo data (See Col. 20, L. 13-47, Col. 22, L. 35-50 and Col. 25, L. 6-39 and the Summary of Nakane et al., wherein it teaches determining the polarity according to the servo data, and hence it controls the polarity reversal circuit in order to process the waveform in order to reproduce the signal.).

Regarding Claim 2, Nakane et al. teaches all the limitations of Claim 1. Nakane et al. further teaches wherein the circuit is operable to recover a servo-synchronization mark from the

servo signal and the determinator is operable to determines the connection polarity from the recovered servo-synchronization mark (Col. 22, L. 36-49 and Col. 24 L. 57 to Col. 25, L. 39).

Regarding Claim 3, Nakane et al. teaches all the limitations of Claim 1. Nakane et al. further teaches wherein the determinator is operable to generate a signal that indicates the determined connection polarity (Col. 22, L. 36-49 and Col. 24 L. 57 to Col. 25, L. 39).

Regarding Claim 5, Nakane et al. teaches all the limitations of Claim 1. Nakane et al. further teaches wherein the circuit is operable to recover the servo data from the servo signal regardless of the connection polarity (Col. 22, L. 36-49 and Col. 24 L. 57 to Col. 25, L. 39, wherein Nakane et al. teaches recovering the connection polarity without emphasizing to which polarity it is, hence is determines it regardless of the connection polarity.).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 4, 21-23, 27, 30, 32, 33, 37, 38, 49 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakane et al. in view of Hayami (US Patent No. 6, 477, 125).

Regarding Claim 4, Nakane et al. teaches all the limitations of Claim 1. Nakane et al., however, does not explicitly teach wherein the detector is a viterbi detector. This limitation is taught by Hayami in which it teaches a Viterbi detector that is able to extract synchronization information according the signal from the bit stream from the received values as taught in Col. 2, L. 25-42. It would have been obvious to a person of ordinary skill in the art, at the time the

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invention was made, to modify Nakane et al.'s invention with the teaching of Hayami in order to minimize the equalization error as taught by Hayami in the Summary of the Invention.

Claim (21) has limitations similar to those treated in the above rejection, and is met by the references as discussed above (i.e. Nakane et al.). Claim (21) however also recites the following limitations: "a Viterbi detector to recover a synchronization mark from samples of a servo signal generated by a read head that is coupled to the Viterbi detector with a connection polarity". However, Nakane et al. does not explicitly teach that the detector is a Viterbi detector. This is taught by Hayami in Col. 2, L. 25-42. It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Nakane et al.'s invention with the teaching of Hayami in order to minimize the equalization error as taught by Hayami in the Summary of the Invention.

Claims (27, 33 and 37) have limitations similar to those treated in the above rejection, and is met by the references as discussed above in Claim 21 under the combination of Nakane et al. and Hayami. Claims (27, 33 and 37) however also recite the following limitations: "a sampling circuit (See Col. 2, L. 53-67 of Nakane et al.) and a comparator coupled to the Viterbi detector and operable to determine the phase of the servo signal from the recovered synchronization mark (See Col. 2, L. 23-26 of Nakane et al., wherein a PLL is disclosed, it is well known in the art that the PLL circuit detects the phase of the readback signals.)".

Method claims (38, 49 and 50) are drawn to the method of using the corresponding apparatus claimed in claim (27). Therefore method claims (38, 49 and 50) correspond to apparatus claim (27) and are rejected for the same reasons of obviousness as used above.

Regarding Claim 22, the combination of Nakane et al. and Hayami teaches all the limitations of Claim 21. The combination further teaches wherein the determinator is operable to generate a signal that indicates the determined connection polarity (Col. 22, L. 36-49 and Col. 24 L. 57 to Col. 25, L. 39 of Nakane et al.).

Regarding Claim 23, the combination of Nakane et al. and Hayami teaches all the limitations of Claim 21. The combination further teaches wherein the circuit is operable to recover the servo data from the servo signal regardless of the connection polarity (Col. 22, L. 36-49 and Col. 24 L. 57 to Col. 25, L. 39, wherein Nakane et al. teaches recovering the connection polarity without emphasizing to which polarity it is, hence is determines it regardless of the connection polarity.).

Regarding Claim 30, the combination of Nakane et al. and Hayami teaches all the limitation of CLaim 27. The combination further teach a sampling circuit (See Col. 2, L. 53-67 of Nakane et al.) and a comparator coupled to the Viterbi detector and operable to determine the phase of the servo signal from the recovered synchronization mark (See Col. 2, L. 23-26 of Nakane et al., wherein a PLL is disclosed, it is well known in the art that the PLL circuit detects the phase of the readback signals.).

Regarding Claim 32, the combination of Nakane et al. and Hayami teaches all the limitations of Claim 27. The combination further teach that the servo signal has other servo data other than the synchronization mark (It is well known in the art that servo data comprises with data other than the synchronization mark. See also Background of Nakane et al.) and a Viterbi

detector coupled to the sampling circuit and operable to recover the other servo data from the samples of the servo signal (Col. 2, L. 25-42 of Hayami).

7. Claims 24, 28, 35 and 39-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakane et al. and Hayami as applied to claims 21 and 27 above, and further in view of Tuttle et al. (US Patent No. 6, 108, 151).

Regarding Claims 24 and 35, the combination of Nakane et al. and Hayami teach all the limitations of Claims 21 and 33. However the combination does not explicitly teach the following:

The synchronization mark has pairs and only pairs of consecutive logic 0's and logic 1's;

And the Viterbi detector comprises,

A recovery circuit operable to recover the synchronization mark from the samples of the servo signal by,

Calculating a respective path metric for each of no more than two possible states of the binary sequence and determining a surviving path from the calculated path metrics, the binary sequence lying along the surviving path.

However, Tuttle teaches these limitations in the synchronization pairs in Col. 8, Lines 48-51 and Lines 56-59 (Tuttle et al. further teach that the read data is binary data.) and the Viterbi detector with a recovery circuit as Claimed in Col. 4, Lines 54-67 and Col. 7, Lines 33-38 and Col. 9, Lines 50-59 (Tuttle et al. teach a circuit that receives inputted data from the head and detects the polarity of the servo signal from that data) and the path metric calculation in Col. 13, Lines 1-60, wherein Tuttle et al. teaches the sampling and coding and processing of code pairs 00, 10, 01, 11. Tuttle et al. teaches determining the path by the use of sampling and further processing of a 2T

preamble. It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify the combination's invention with the teaching of Tuttle et al. in order to synchronize the servo data according to the polarity being read by the head device.

Regarding Claim 28, the combination of Osada and Reed et al. teach all the limitations of Claim 27. However, the combination does not teach the comparator is coupled to the sampling circuit and the sampling circuit is operable to generate the samples of the servo signal having a desired phase. Tuttle teaches this in Col. 8, Lines 48-51 and Lines 56-59 and Col. 19, Line 65 to Col. 20, Line 11 (Tuttle et al. teaches that the device detects if the desired pulse is positive or negative.).

Regarding Claim 39, the combination of Osada and Reed et al. all the limitations of Claim 38. The combination does teach determining comprises determining the phase of the servo signal from the recovered synchronization mark (See Fig. 7 along with description, wherein it determines which is the direction of the polarity of the signal and wherein it inverts the polarity if required.). However, the combination does not explicitly teach wherein the servo data includes a synchronization mark. Tuttle et al. teaches this limitation in Col. 12, Lines 5-8.

8. Claims 29, 31 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Nakane et al. and Hayami as applied to claim 27 and 33 above, and further in view of Osada (US Patent No. 5, 291, 464).

Regarding Claims 29 and 34, the combination teach all the limitations of Claims 27 and 33. However, the combination does not explicitly teach wherein the comparator is coupled to the sampling circuit and if the determined phase is opposite to a desired phase, then the sampling circuit is operable to invert the samples of the servo signal. Osada teaches in the Abstract that the

signals are sampled (see also Summary of the Invention, wherein it describes both servo signals and a procedure with how they use the phases in order to compare and invert its polarity and it teaches inverting the samples according to the detection.). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify the combination's invention with the teaching of Osada in order to prevent undetected phase changes.

Regarding 31, the combination teach all the limitations of Claims 27 and 33. However, the combination does not explicitly teach wherein the phase of the servo signal represents a connection polarity between the sampling circuit and a read head that generates the servo signal. This is taught by Osada in Fig. 7 and Abstract and Summary of the Invention.

9. Claims 25, 26 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakane et al. and Hayami as applied to claims 21 and 38 above, and further in view of Cloke (US Patent No. 5, 822, 143).

Regarding Claims 25, 26 and 42, the combination teaches all the limitations of Claims 21 and 38. However, the combination does explicitly teach wherein the determining comprises, comparing the recovered synchronization mark to an ideal synchronization mark on a bit-by-bit basis, determining that the servo signal is in phase if the number of mismatching bits is less than or equal to a first predetermined threshold, and determining that the servo signal is out of phase if the number of mismatching bits is greater than or equal to a second predetermined threshold. Cloke et al. teaches this limitations in Fig. 1A and Col. 1, Lines 45-48, Lines 53-59 and Col. 1, Line 60 to Col. 2, Line 19. It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify the combination's invention with the teaching of

Cloke et al. to use a path metric in order to effectively estimate the most likely sequence of symbols.

Response to Arguments

10. Applicant's arguments filed 10/16/06 have been fully considered but they are not persuasive. Applicant Argues that "Nakane, on the other hand, does not disclose a read-write head coupled to the circuit with a connection polarity, and a determinator operable to determine the connection polarity from the recovered servo data." Examiner does not concur with the Applicant because Nakane's invention does illustrate a read write head in Element 107, being connected to a polarity reversal circuit which detects and determines the polarity as it is explained in Col. 20, L. 13-47, which is what the connection polarity does according the Applicant Specification in Pages 9-13, wherein the connection polarity determines the polarity of the head and determines if the polarity is not the same as the head polarity and hence proceeds to compensate for the discrepancy. Applicant also argues: "Nakane does not teach any kind of magnetic data-storage device". However, "magnetic data-storage" is not used in any of the independent claims. Therefore, the Claims remain rejected under the previous rejection.

11. After further reconsideration, Claim 36 rejection under 112 first paragraph has been withdrawn.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO**

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MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenda P. Rodriguez whose telephone number is (571) 272-7561. The examiner can normally be reached on Monday thru Thursday: 7:00-5:00; alternate Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrea L. Wellington can be reached on (571) 272-4483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


gpr
TAN DINH
PRIMARY EXAMINER

1/24/07